gain and is different for the positive and negative supplies. The offset change referred-to-input (RTI) is usually specified in dB form. For example, a PSR of 100dB at a gain of 1000 would imply an input-offset-voltage change of 10μV-per-volt of power supply change. The output offset change-per-volt of power-supply change would be 10mV. PSR in the specification tables is measured at DC.

Input Bias Current — The input bias currents are currents flowing into (or out of) the two inputs of the amplifier. The value given in the specification table is the maximum current into either input. Input offset current is the difference between the two input bias currents.

Input Voltage Range — The linear operating range of the amplifier is referred to as the "input voltage range". When operating at high gains with small differential inputs, this input range is the common-mode input voltage range.

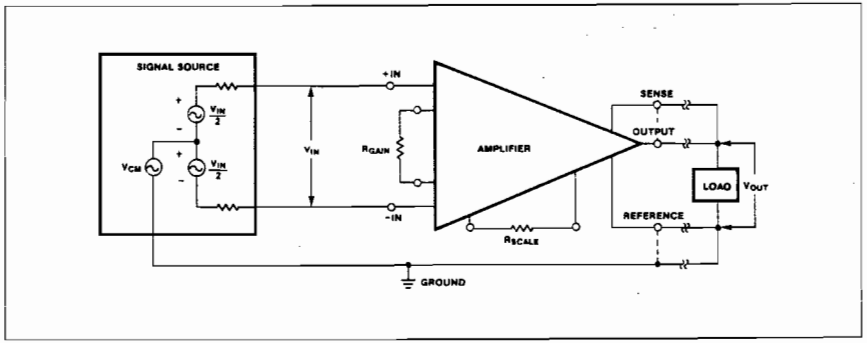
Common-Mode Rejection — Common-mode rejection (CMR) specifies the amplifiers ability to reject common-mode inputs. The ratio of change in output voltage to a change in common-mode input voltage is the common-mode gain ($\Delta V_O/\Delta V_{CM}$). The ratio of differential gain (G) to common-mode gain (A_{CM}) is defined as common-mode rejection ratio (CMRR). The CMR is conventionally specified in log form; CMR = 20 $\log_{10}$ CMRR.

Since instrumentation amplifiers are designed to amplify differential signals while rejecting common-mode inputs, common-mode gain stays essentially independent of gain setting. Therefore, CMRR increases almost directly with the gain setting.

As an example, consider a CMR of 120dB at a gain of 1000 with a common-mode input range of ±10V. The 120dB of CMR implies a CMRR of 1000/A_{CM} = 1,000,000, or a common-mode gain of 1/1000. A ±10V common-mode input will cause an output change of ±10mV for this example (CMR = 120dB, G = 1000).

Gain Equation Accuracy — Differential gain is given as a function of one or two external resistors. The specified accuracy limits indicate the accuracy of the amplifier given an exact ratio of gain setting resistors R_S and R_G, when two resistors are used, or an exact value of R_G when only one resistor is used.

INSTRUMENTATION AMPLIFIER FUNCTIONAL DIAGRAM



FX 24.19 EX 33.71 JOE BUCKSON, 408 727-9222

AMP-01
LOW-NOISE
PRECISION INSTRUMENTATION AMPLIFIER

FEATURES

- **Low Offset Voltage** ..... **50μV Max**
- **Very Low Offset Voltage Drift** ..... **0.3μV/°C Max**
- **Low Noise** ..... **0.12μV_{p-p} (0.1Hz to 10Hz)**
- **Excellent Output Drive** ..... **±10V at ±50mA**
- **Capacitive Load Stability** ..... **to 1μF**
- **Gain Range** ..... **0.1 to 10,000**
- **Excellent Linearity** ..... **16-Bit at G = 1000**
- **High CMR** ..... **125dB Min (G = 1000)**
- **Low Bias Current** ..... **4nA Max**
- **May be Configured as a Precision Op-Amp**
- **Output-Stage Thermal Shutdown**
- **Available in Die Form**

ORDERING INFORMATION†

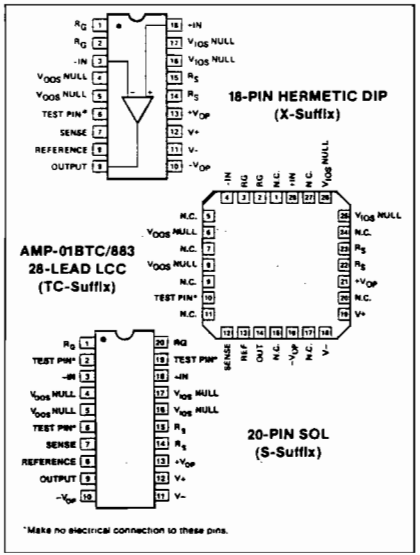
PACKAGE			OPERATING TEMPERATURE RANGE
CERDIP 18-PIN	LCC	PLASTIC 20-PIN	
AMP01AX*	—	—	MIL
AMP01BX*	AMP01BTC/883	—	MIL
AMP01EX	—	—	IND
AMP01FX	—	—	IND
—	—	AMP01GS††	COM

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

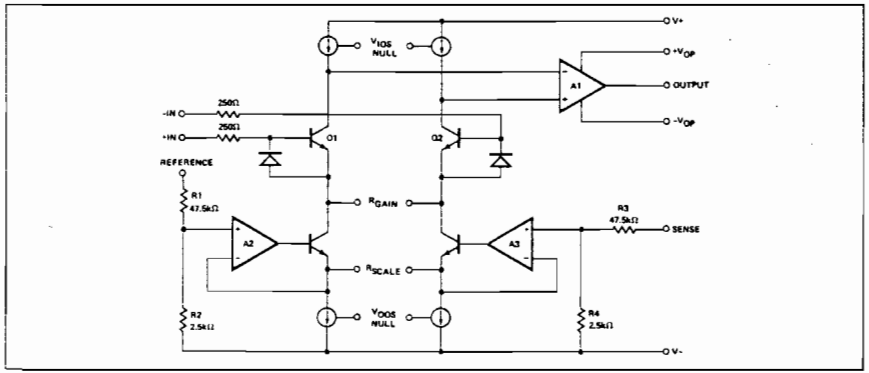
† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages. For ordering information, see 1990/91 Data Book, Section 2.

†† For availability and burn-in information on SO and PLCC packages, contact your local sales office.

PIN CONNECTIONS



SIMPLIFIED SCHEMATIC



Manufactured under the following U.S. patents: 4,471,321 and 4,503,381.

GENERAL DESCRIPTION

The AMP-01 is a monolithic instrumentation amplifier designed for high-precision data acquisition and instrumentation applications. The design combines the conventional features of an instrumentation amplifier with a high-current output stage. The output remains stable with high capacitance loads (1μF), a unique ability for an instrumentation amplifier. Consequently, the AMP-01 can amplify low-level signals for transmission through long cables without requiring an output buffer. The output stage may be configured as a voltage or current generator.

Input offset voltage is very low (20μV) which generally eliminates the external null potentiometer. Temperature changes have minimal effect on offset; TCV_{IOS} is typically 0.15μV/°C. Excellent low-frequency noise performance is achieved with a minimal compromise on input protection. Bias current is very low, less than 10nA over the military temperature range. High common-mode rejection of 130dB, 16-bit linearity at a gain of 1000, and 50mA peak output current are achievable simultaneously. This combination takes the instrumentation amplifier one step further towards the ideal amplifier.

AC performance complements the superb DC specifications. The AMP-01 slews at 4.5V/μs into capacitive loads of up to 15nF, settles in 50μs to 0.01% at a gain of 1000, and boasts a healthy 26MHz gain-bandwidth product. These features make the AMP-01 ideal for high-speed data-acquisition systems.

Gain is set by the ratio of two external resistors over a range of 0.1 to 10,000. A very low gain-temperature-coefficient of 10ppm/°C is achievable over the whole gain range. Output voltage swing is guaranteed with three load resistances; 50Ω, 500Ω, and 2kΩ. Loaded with 500Ω, the output delivers ±13.0V minimum. A thermal shutdown circuit prevents destruction of the output transistors during overload conditions.

The AMP-01 can also be configured as a high-performance operational amplifier. In many applications, the AMP-01 can be used in place of op-amp/power-buffer combinations.

THEORY OF OPERATION

An instrumentation amplifier, unlike an op amp, requires precise internal feedback. The two techniques presently in use are resistive and current feedback.

The AMP-01 employs the current feedback approach which has significant advantages over resistive feedback. Advantages of current-feedback are:

a. The technique yields a very high common-mode rejection ratio. The AMP-01 CMR is in excess of 130dB at a gain of 1000.

b. The gain of the current feedback design is set by the ratio of two external resistors. Using external resistors allows any practical gain to be set with high precision and very low gain temperature coefficient.

c. The current-feedback design is immune to CMR degradation when series resistance is added to the reference input. A small (trimmable) offset change results from added resistance, e.g. a printed circuit track.

The AMP-01 utilizes low-drift thin-film resistors to minimize output offset temperature drift. A feedback voltage-to-current converter is employed having high linearity and low noise, particularly at low frequencies. Parameter shifts during packaging are eliminated by a post-assembly trimming technique which electronically adjusts the output offset voltage.

The AMP-01 input transistors Q1 and Q2 feed active loads, yielding stage gain in excess of 4000 (see simplified schematic). The output amplifier, A1, is a two-stage design having a gain of about 50,000 driving a 100Ω load. Overall gain of 2×10^8 yields excellent linearity, even at high closed-loop gains.

Low bias current is achieved by using ion-implanted superbeta transistors combined with a new bias-current cancellation system, patents applied for. Input bias current remains below 10nA over the military temperature range, −55°C to +125°C.

Superbeta transistors use a new transistor geometry resulting in an input noise of only $5nV/\sqrt{Hz}$ at G = 1000. Noise includes contributions from the gain-setting resistor and internal overload-protection resistor. The input stage achieves an offset voltage drift of less than 0.3μV/°C (E Grade).

The AMP-01 uses a unique two-pole compensation scheme where the load capacitance is incorporated into the dominate pole. Stable operation results even with high capacitance loads. The high output current capability (90mA peak) allows the 4.5V/μs slew-rate to be maintained with load capacitance as high as 15nF.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage ..... ±18V
Common-Mode Input Voltage ..... Supply Voltage
Differential Input Voltage, $R_G \geq 2k\Omega$ ..... ±20V
$R_F < 2k\Omega$ ..... ±10V
Output Short-Circuit Duration ..... Indefinite
Storage Temperature Range ..... −65°C to +150°C
Operating Temperature Range
AMP-01A, B ..... −55°C to +125°C
AMP-01E, F ..... −25°C to +85°C
AMP-01G ..... 0°C to +70°C
Lead Temperature (Soldering, 60 sec) ..... 300°C
Junction Temperature (T_J) ..... −65°C to +150°C

PACKAGE TYPE	Θ_{JA} (Note 2)	Θ_{JC}	UNITS
18-Pin Hermetic DIP (Z)	79	11	°C/W
28-Contact LCC (TC)	78	30	°C/W
20-Pin SOL (S)	88	25	°C/W

NOTES:
1. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
2. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for CerDIP and LCC packages; Θ_{JA} is specified for device soldered to printed circuit board for SOL package.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $R_S = 10k\Omega$, $R_L = 2k\Omega$, $T_A = 25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	AMP-01A MIN	AMP-01A TYP	AMP-01A MAX	AMP-01B MIN	AMP-01B TYP	AMP-01B MAX	UNITS
OFFSET VOLTAGE									
Input Offset Voltage	V_{IOS}	$T_A = 25°C$	—	20	50	—	40	100	μV
		$-55°C \leq T_A \leq +125°C$	—	40	60	—	60	150	
Input Offset Voltage Drift	TCV_{IOS}	$-55°C \leq T_A \leq +125°C$	—	0.15	0.3	—	0.3	1.0	μV/°C
Output Offset Voltage	V_{OOS}	$T_A = 25°C$	—	1	3	—	2	6	mV
		$-55°C \leq T_A \leq +125°C$	—	3	6	—	6	10	
Output Offset Voltage Drift	TCV_{OOS}	$R_G = \infty$ $-55°C \leq T_A \leq +125°C$	—	20	50	—	50	120	μV/°C
Offset Referred to Input vs. Positive Supply $V+ = +5V$ to $+15V$	PSR	G = 1000	120	130	—	110	120	—	dB
		G = 100	110	130	—	100	120	—	
		G = 10	95	110	—	90	100	—	
		G = 1	75	90	—	70	80	—	
		$-55°C \leq T_A \leq +125°C$							
		G = 1000	120	130	—	110	120	—	dB
		G = 100	110	130	—	100	120	—	
		G = 10	95	110	—	90	100	—	
		G = 1	75	90	—	70	80	—	
Offset Referred to Input vs. Negative Supply $V- = -5V$ to $-15V$	PSR	G = 1000	105	125	—	105	115	—	dB
		G = 100	90	105	—	90	95	—	
		G = 10	70	85	—	70	75	—	
		G = 1	50	65	—	50	60	—	
		$-55°C \leq T_A \leq +125°C$							
		G = 1000	105	125	—	105	115	—	dB
		G = 100	90	105	—	90	95	—	
		G = 10	70	85	—	70	75	—	
		G = 1	50	65	—	50	60	—	
Input Offset Voltage Trim Range		$V_S = \pm 4.5V$ to $\pm 18V$ (Note 1)	—	±6	—	—	±6	—	mV
Output Offset Voltage Trim Range		$V_S = \pm 4.5V$ to $\pm 18V$ (Note 1)	—	±100	—	—	±100	—	mV
INPUT CURRENT									
Input Bias Current	I_B	$T_A = 25°C$	—	1	4	—	2	6	nA
		$-55°C \leq T_A \leq +125°C$	—	4	10	—	6	15	
Input Bias Current Drift	TCI_B	$-55°C \leq T_A \leq +125°C$	—	40	—	—	50	—	pA/°C
Input Offset Current	I_{OS}	$T_A = 25°C$	—	0.2	1.0	—	0.5	2.0	nA
		$-55°C \leq T_A \leq +125°C$	—	0.5	3.0	—	1.0	6.0	
Input Offset Current Drift	TCI_{OS}	$-55°C \leq T_A \leq +125°C$	—	3	—	—	5	—	pA/°C
INPUT									
Input Resistance	R_{IN}	Differential, G = 1000	—	1	—	—	1	—	GΩ
		Differential, G ≤ 100	—	10	—	—	10	—	
		Common-Mode, G = 1000	—	20	—	—	20	—	
Input Voltage Range	IVR	$T_A = 25°C$ (Note 2)	±10.5	—	—	±10.5	—	—	V
		$-55°C \leq T_A \leq +125°C$	±10.0	—	—	±10.0	—	—	
Common-Mode Rejection	CMR	$V_{CM} = \pm 10V$, 1kΩ source imbalance							
		G = 1000	125	130	—	115	125	—	dB
		G = 100	120	130	—	110	125	—	
		G = 10	100	120	—	95	110	—	
		G = 1	85	100	—	75	90	—	
		$-55°C \leq T_A \leq +125°C$							
		G = 1000	120	125	—	110	120	—	dB
		G = 100	115	125	—	105	120	—	
		G = 10	95	115	—	90	105	—	
		G = 1	80	95	—	75	90	—	

NOTES:
1. V_{IOS} and V_{OOS} nulling has minimal affect on TCV_{IOS} and TCV_{OOS}, respectively.
2. Refer to section on common-mode rejection.

ELECTRICAL CHARACTERISTICS at $V_S = \pm15V$, $R_S = 10k\Omega$, $R_L = 2k\Omega$, $T_A = +25°C$, $-25°C \le T_A \le +85°C$ for E,F grades, $0°C \le T_A \le +70°C$ for G grade, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	AMP-01E MIN	AMP-01E TYP	AMP-01E MAX	AMP-01F/G MIN	AMP-01F/G TYP	AMP-01F/G MAX	UNITS
OFFSET VOLTAGE									
Input Offset Voltage	V_{IOS}	$T_A = +25°C$	–	20	50	–	40	100	µV
		$T_{MIN} \le T_A \le T_{MAX}$	–	40	60	–	80	150	
Input Offset Voltage Drift	TCV_{IOS}	$T_{MIN} \le T_A \le T_{MAX}$ (Note 2)	–	0.15	0.3	–	0.3	1.0	µV/°C
Output Offset Voltage	V_{OOS}	$T_A = +25°C$	–	1	3	–	2	6	mV
		$T_{MIN} \le T_A \le T_{MAX}$	–	3	6	–	6	10	
Output Offset Voltage Drift	TCV_{OOS}	RG = – (Note 2)	–	20	100	–	50	120	µV/°C
		$T_{MIN} \le T_A \le T_{MAX}$							
Offset Referred to Input vs. Positive Supply V+ = +5V to +15V	PSR	G = 1000	120	130	–	110	120	–	dB
		G = 100	110	130	–	100	120	–	
		G = 10	95	110	–	90	100	–	
		G = 1	75	90	–	70	80	–	
		$T_{MIN} \le T_A \le T_{MAX}$ G = 1000	120	130	–	110	120	–	dB
		G = 100	110	130	–	100	120	–	
		G = 10	95	110	–	90	100	–	
		G = 1	75	90	–	70	80	–	
Offset Referred to Input vs. Negative Supply V– = –5V to –15V	PSR	G = 1000	110	125	–	105	115	–	dB
		G = 100	95	105	–	90	95	–	
		G = 10	75	85	–	70	75	–	
		G = 1	55	65	–	50	60	–	
		$T_{MIN} \le T_A \le T_{MAX}$ G = 1000	110	125	–	105	115	–	dB
		G = 100	95	105	–	90	95	–	
		G = 10	75	85	–	70	75	–	
		G = 1	55	65	–	50	60	–	
Input Offset Voltage Trim Range		$V_S = \pm4.5V$ to $\pm18V$ (Note 1)	–	±6	–	–	±6	–	mV
Output Offset Voltage Trim Range		$V_S = \pm4.5V$ to $\pm18V$ (Note 1)	–	±100	–	–	±100	–	mV
INPUT CURRENT									
Input Bias Current	I_B	$T_A = +25°C$	–	1	4	–	2	6	mV
		$T_{MIN} \le T_A \le T_{MAX}$	–	4	10	–	6	15	
Input Bias Current Drift	TCI_B	$T_{MIN} \le T_A \le T_{MAX}$	–	40	–	–	50	–	pA/°C
Input Offset Current	I_B	$T_A = +25°C$	–	0.2	1.0	–	0.5	2.0	mV
		$T_{MIN} \le T_A \le T_{MAX}$	–	0.5	3.0	–	1.0	6.0	
Input Offset Current Drift	TCI_{OS}	$T_{MIN} \le T_A \le T_{MAX}$	–	3	–	–	5	–	pA/°C
INPUT									
Input Resistance	R_{IN}	Differential, G = 1000	–	1	–	–	1	–	GΩ
		Differential, G ≤ 100	–	10	–	–	10	–	
		Common-Mode, G = 1000	–	20	–	–	20	–	
Input Voltage Range	IVR	$T_A = +25°C$ (Note 3)	±10.5	–	–	±10.5	–	–	V
		$T_{MIN} \le T_A \le T_{MAX}$	±10.0	–	–	±10.0	–	–	
Common-Mode Rejection	CMR	$V_{CM} = \pm10V$, 1kΩ source imbalance							
		G = 1000	125	130	–	115	125	–	dB
		G = 100	120	130	–	110	125	–	
		G = 10	100	120	–	95	110	–	
		G = 1	85	100	–	75	90	–	
		$T_{MIN} \le T_A \le T_{MAX}$ G = 1000	120	125	–	110	120	–	dB
		G = 100	115	125	–	105	120	–	
		G = 10	95	115	–	90	105	–	
		G = 1	80	95	–	75	90	–	

NOTES:
1. V_{IOS} and V_{OOS} nulling has minimal effect on TCV_{IOS} and TCV_{OOS}, respectively.
2. Sample tested.
3. Refer to section on common-mode rejection.

ELECTRICAL CHARACTERISTICS at $V_S = \pm15V$, $R_S = 10k\Omega$, $R_L = 2k\Omega$, $T_A = 25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	AMP-01A/E MIN	AMP-01A/E TYP	AMP-01A/E MAX	AMP-01B/F/G MIN	AMP-01B/F/G TYP	AMP-01B/F/G MAX	UNITS
GAIN									
Gain Equation Accuracy		$G = \frac{20 \times R_S}{R_G}$ Accuracy Measured from G = 1 to 1000	–	0.3	0.6	–	0.5	0.8	%
Gain Range	G		0.1	–	10k	0.1	–	10k	V/V
Nonlinearity		G = 1000	–	0.0007	0.005	–	0.0007	0.005	%
		G = 100	–	–	0.005	–	–	0.005	
		G = 10 (Note 1)	–	–	0.005	–	–	0.007	
		G = 1	–	–	0.010	–	–	0.015	
Temperature Coefficient	G_{TC}	$1 \le G \le 1000$ (Notes 1, 2)	–	5	10	–	5	15	ppm/°C
OUTPUT RATING									
Output Voltage Swing	V_{OUT}	$R_L = 2k\Omega$	±13.0	±13.8	–	±13.0	±13.8	–	V
		$R_L = 500\Omega$	±13.0	±13.5	–	±13.0	±13.5	–	
		$R_L = 50\Omega$	±2.5	±4.0	–	±2.5	±4.0	–	
		$R_L = 2k\Omega$ Over Temp.	±12.0	±13.8	–	±12.0	±13.8	–	V
		$R_L = 500\Omega$ (Note 3)	±12.0	±13.5	–	±12.0	±13.5	–	
Positive Current Limit		Output-to-Ground Short	60	100	120	60	100	120	mA
Negative Current Limit		Output-to-Ground Short	60	90	120	60	90	120	mA
Capacitive Load Stability		$1 \le G \le 1000$ No Oscillations. (Note 1)	0.1	1	–	0.1	1	–	µF
Thermal Shutdown Temperature		Junction Temperature	–	185	–	–	165	–	°C
NOISE									
Voltage Density, RTI	e_n	$f_O = 1kHz$							nV/√Hz
		G = 1000	–	5	–	–	5	–	
		G = 100	–	10	–	–	10	–	
		G = 10	–	59	–	–	59	–	
		G = 1	–	540	–	–	540	–	
Noise Current Density, RTI	i_n	$f_O = 1kHz$, G = 1000	–	0.15	–	–	0.15	–	pA/√Hz
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz							µV p-p
		G = 1000	–	0.12	–	–	0.12	–	
		G = 100	–	0.18	–	–	0.18	–	
		G = 10	–	1.4	–	–	1.4	–	
		G = 1	–	13	–	–	13	–	
Input Noise Current	i_{np-p}	0.1Hz to 10Hz, G = 1000	–	2	–	–	2	–	pA p-p
DYNAMIC RESPONSE									
Small-Signal Bandwidth (–3dB)	BW	G = 1	–	570	–	–	570	–	kHz
		G = 10	–	100	–	–	100	–	
		G = 100	–	82	–	–	82	–	
		G = 1000	–	26	–	–	26	–	
Slew Rate	SR	G = 10	3.5	4.5	–	3.0	4.5	–	V/µs
Settling Time	t_S	To 0.01%, 20V step							µs
		G = 1	–	12	–	–	12	–	
		G = 10	–	13	–	–	13	–	
		G = 100	–	15	–	–	15	–	
		G = 1000	–	50	–	–	50	–	

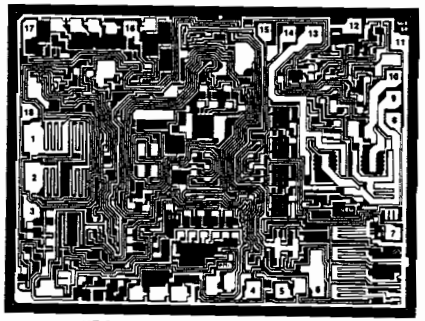
NOTES:
1. Guaranteed by design.
2. Gain tempco does not include the effects of gain and scale resistor tempco match.
3. $-55°C \le T_A \le +125°C$ for A/B grades, $-25°C \le T_A \le +85°C$ for E/F grades, $0°C \le T_A \le 70°C$ FOR G grades.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $R_S = 10k\Omega$, $R_L = 2k\Omega$, $T_A = 25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	AMP-01A/E MIN	AMP-01A/E TYP	AMP-01A/E MAX	AMP-01B/F/G MIN	AMP-01B/F/G TYP	AMP-01B/F/G MAX	UNITS
SENSE INPUT									
Input Resistance	R_{IN}		35	50	65	35	50	65	kΩ
Input Current	I_{IN}	Referenced to V−	—	280	—	—	280	—	μA
Voltage Range		(Note 1)	−10.5	—	+15	−10.5	—	+15	V
REFERENCE INPUT									
Input Resistance	R_{IN}		35	50	65	35	50	65	kΩ
Input Current	I_{IN}	Referenced to V−	—	280	—	—	260	—	μA
Voltage Range		(Note 1)	−10.5	—	+15	−10.5	—	+15	V
Gain to Output			—	1	—	—	1	—	V/V
POWER SUPPLY $-25°C \le T_A \le -85°C$ for E/F Grades, $-55°C \le T_A \le -125°C$ for A/B Grades									
Supply Voltage Range	V_S	+V linked to $+V_{OP}$ −V linked to $-V_{OP}$	±4.5	—	±18	±4.5	—	±18	V
Quiescent Current	I_Q	+V linked to $+V_{OP}$	—	3.0	4.8	—	3.0	4.6	mA
		−V linked to $-V_{OP}$	—	3.4	4.8	—	3.4	4.8	

NOTE:
1. Guaranteed by design.

DICE CHARACTERISTICS



DIE SIZE 0.111 × 0.149 inch, 16,539 sq. mils
(2.82 × 3.78 mm, 10.67 sq. mm)

1. R_G
2. R_G
3. −INPUT
4. V_{OOS} NULL
5. V_{OOS} NULL
6. TEST PIN*
7. SENSE
8. REFERENCE
9. OUTPUT
10. V− (OUTPUT)
11. V−
12. V+
13. V+ (OUTPUT)
14. R_S
15. R_S
16. V_{IOS} NULL
17. V_{IOS} NULL
18. +INPUT

*Make no electrical connection

For additional DICE ordering information, refer to PMI's Data Book, Section 2.

WAFER TEST LIMITS at $V_S = \pm 15V$, $R_S = 10k\Omega$, $R_L = 2k\Omega$, $T_A = 25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	AMP-01NBC LIMIT	AMP-01GBC LIMIT	UNITS
Input Offset Voltage	V_{IOS}		60	120	μV MAX
Output Offset Voltage	V_{OOS}		4	8	mV MAX
Offset Referred to Input vs. Positive Supply	PSR	V+ = +5V to +15V G = 1000	120	110	dB MIN
		G = 100	110	100	
		G = 10	95	90	
		G = 1	75	70	
Offset Referred to Input vs. Negative Supply	PSR	V− = −5V to −15V G = 1000	105	105	dB MIN
		G = 100	90	90	
		G = 10	70	70	
		G = 1	50	50	
Input Bias Current	I_B		4	8	nA MAX
Input Offset Current	I_{OS}		1	3	nA MAX
Input Voltage Range	IVR	Guaranteed by CMR Tests	±10	±10	V MIN
Common-Mode Rejection	CMR	$V_{CM} = \pm 10V$ G = 1000	125	115	dB MIN
		G = 100	120	110	
		G = 10	100	95	
		G = 1	85	75	
Gain Equation Accuracy		$G = \frac{20 \times R_S}{R_G}$	0.6	0.8	% MAX
Output Voltage Swing	V_{OUT}	$R_L = 2k\Omega$	±13	±13	V MIN
		$R_L = 500\Omega$	±13	±13	
		$R_L = 50\Omega$	±2.5	±2.5	
Output-Current Limit		Output-to-Ground Short	±60	±60	mA MIN
Output-Current Limit		Output-to-Ground Short	±120	±120	mA MAX
Quiescent Current	I_Q	+V Linked to $+V_{OP}$ −V Linked to $-V_{OP}$	4.8	4.8	mA MAX

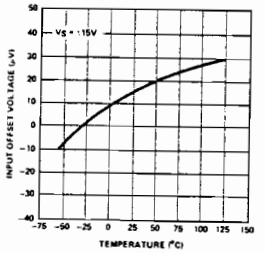
NOTE:
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $R_S = 10k\Omega$, $R_L = 2k\Omega$, $T_A = 25°C$, unless otherwise noted.

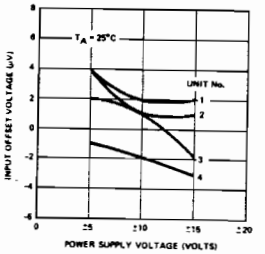
PARAMETER	SYMBOL	CONDITIONS	AMP-01NBC TYPICAL	AMP-01GBC TYPICAL	UNITS
Input Offset Voltage Drift	TCV_{IOS}		0.15	0.30	µV/°C
Output Offset Voltage Drift	TCV_{OOS}	$R_G = \infty$	20	50	µV/°C
Input Bias Current Drift	TCI_B		40	50	pA/°C
Input Offset Current Drift	TCI_{OS}		3	5	pA/°C
Nonlinearity		G = 1000	0.0007	0.0007	%
Voltage Noise Density	e_n	G = 1000 f_O = 1kHz	5	5	nV/√Hz
Current Noise Density	i_n	G = 1000 f_O = 1kHz	0.15	0.15	pA/√Hz
Voltage Noise	e_{np-p}	G = 1000 0.1Hz to 10Hz	0.12	0.12	μV_{p-p}
Current Noise	i_{np-p}	G = 1000 0.1Hz to 10Hz	2	2	pA_{p-p}
Small-Signal Bandwidth (-3dB)	BW	G = 1000	26	26	kHz
Slew Rate	SR	G = 10	4.5	4.5	V/µs
Settling Time	t_S	To 0.01%, 20V Step G = 1000	50	50	µs

TYPICAL PERFORMANCE CHARACTERISTICS

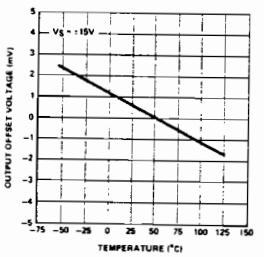
INPUT OFFSET VOLTAGE vs TEMPERATURE



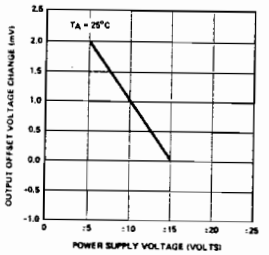
INPUT OFFSET VOLTAGE vs SUPPLY VOLTAGE



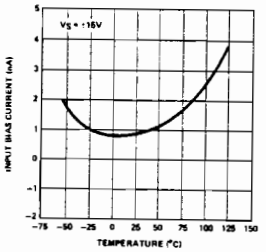
OUTPUT OFFSET VOLTAGE vs TEMPERATURE



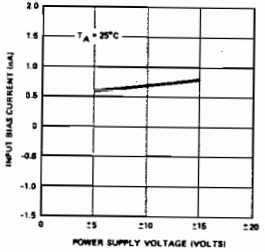
OUTPUT OFFSET VOLTAGE CHANGE vs SUPPLY VOLTAGE



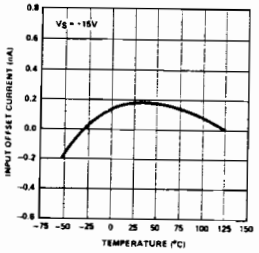
INPUT BIAS CURRENT vs TEMPERATURE



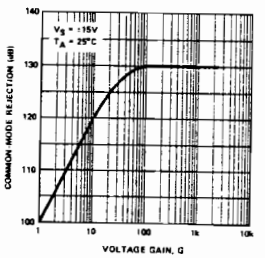
INPUT BIAS CURRENT vs SUPPLY VOLTAGE



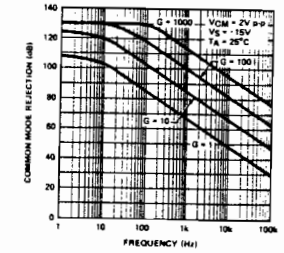
INPUT OFFSET CURRENT vs TEMPERATURE



COMMON-MODE REJECTION vs VOLTAGE GAIN

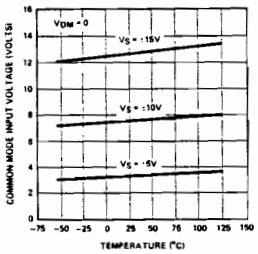


COMMON-MODE REJECTION vs FREQUENCY

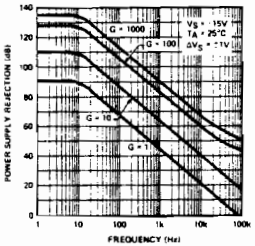


TYPICAL PERFORMANCE CHARACTERISTICS

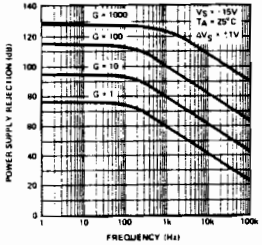
COMMON-MODE VOLTAGE RANGE vs TEMPERATURE



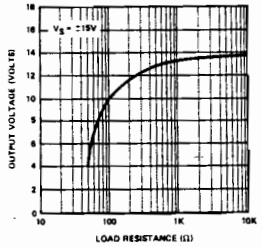
POSITIVE PSR vs FREQUENCY



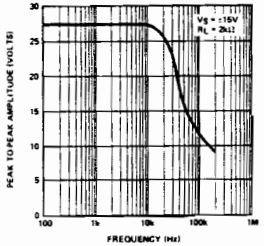
NEGATIVE PSR vs FREQUENCY



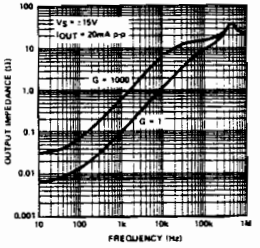
MAXIMUM OUTPUT VOLTAGE vs LOAD RESISTANCE



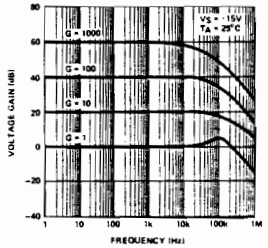
MAXIMUM OUTPUT SWING vs FREQUENCY



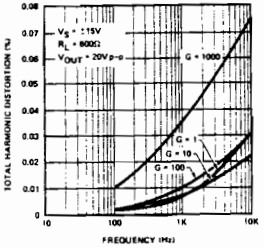
CLOSED-LOOP OUTPUT IMPEDANCE vs FREQUENCY



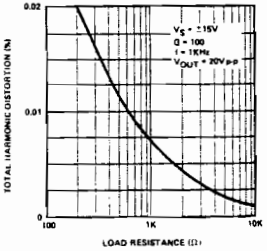
CLOSED-LOOP VOLTAGE GAIN vs FREQUENCY



TOTAL HARMONIC DISTORTION vs FREQUENCY

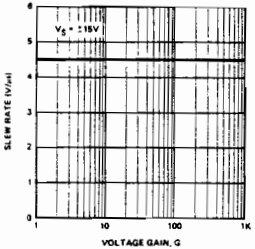


TOTAL HARMONIC DISTORTION vs LOAD RESISTANCE

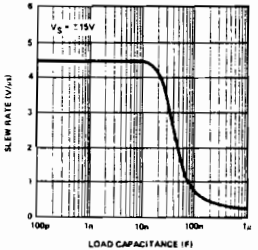


TYPICAL PERFORMANCE CHARACTERISTICS

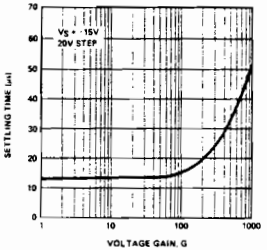
SLEW RATE vs VOLTAGE GAIN



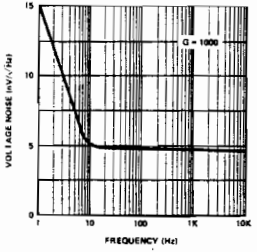
SLEW RATE vs LOAD CAPACITANCE



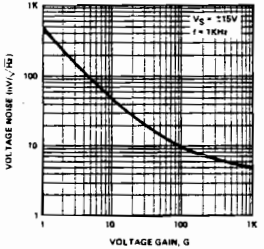
SETTLING TIME TO 0.01% vs VOLTAGE GAIN



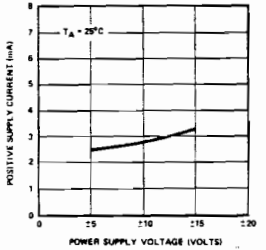
VOLTAGE NOISE DENSITY vs FREQUENCY



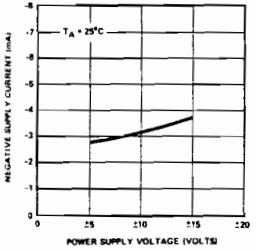
RTI VOLTAGE NOISE DENSITY vs GAIN



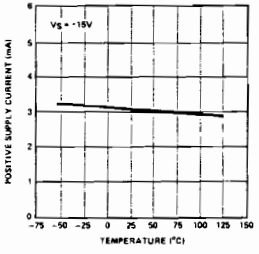
POSITIVE SUPPLY CURRENT vs SUPPLY VOLTAGE



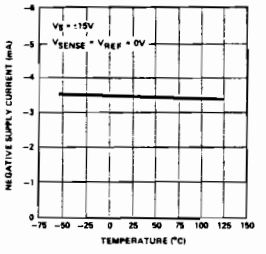
NEGATIVE SUPPLY CURRENT vs SUPPLY VOLTAGE



POSITIVE SUPPLY CURRENT vs TEMPERATURE



NEGATIVE SUPPLY CURRENT vs TEMPERATURE



INPUT AND OUTPUT OFFSET VOLTAGES

Instrumentation amplifiers have independent offset voltages associated with the input and output stages. While the initial offsets may be adjusted to zero, temperature variations will cause shifts in offsets. Systems with auto-zero can correct for offset errors, so initial adjustment would be unnecessary. However, many high-gain applications don't have auto zero. For these applications, both offsets can be nulled, which has minimal effect on TCV_{IOS} and TCV_{OOS}.

The input offset component is directly multiplied by the amplifier gain, whereas output offset is independent of gain. Therefore, at low gain, output-offset-errors dominate, while at high gain, input-offset-errors dominate. Overall offset voltage, V_{OS}, referred to the output (RTO) is calculated as follows;

$$V_{OS}(RTO) = (V_{IOS} \times G) + V_{OOS} \quad \text{(1)}$$

where V_{IOS} and V_{OOS} are the input and output offset voltage specifications and G is the amplifier gain. Input offset nulling alone is recommended with amplifiers having fixed gain above 50. Output offset nulling alone is recommended when gain is fixed at 50 or below.

In applications requiring both initial offsets to be nulled, the input offset is nulled first by short-circuiting R_G, then the output offset is nulled with the short removed.

The overall offset voltage drift TCV_{OS}, referred to the output, is a combination of input and output drift specifications. input offset voltage drift is multiplied by the amplifier gain, G, and summed with the output offset drift;

$$TCV_{OS}(RTO) = (TCV_{IOS} \times G) + TCV_{OOS} \quad \text{(2)}$$

where TCV_{IOS} is the input offset voltage drift, and TCV_{OOS} is the output offset voltage specification. Frequently, the amplifier drift is referred back to the input (RTI) which is then equivalent to an input signal change;

$$TCV_{OS}(RTI) = TCV_{IOS} + \frac{TCV_{OOS}}{G} \quad \text{(3)}$$

For example, the maximum input-referred drift of an AMP-01EX set to G = 1000 becomes;

$$TCV_{OS}(RTI) = 0.3\mu V/°C + \frac{100\mu V/°C}{1000} = 0.4\mu V/°C \text{ max.}$$

INPUT BIAS AND OFFSET CURRENTS

Input transistor bias currents are additional error sources which can degrade the input signal. Bias currents flowing through the signal source resistance appear as an additional offset voltage. Equal source resistance on both inputs of an IA will minimize offset changes due to bias current variations with signal voltage and temperature. However, the difference between the two bias currents, the input offset current, produces a non-trimmable error. The magnitude of the error is the offset current times the source resistance.

A current path must always be provided between the differential inputs and analog ground to ensure correct amplifier operation. Floating inputs, such as thermocouples, should be grounded close to the signal source for best common-mode rejection.

GAIN

The AMP-01 uses two external resistors for setting voltage gain over the range 0.1 to 10,000. The magnitudes of the scale resistor, R_S, and gain-set resistor, R_G, are related by the formula: $G = 20 \times R_S/R_G$, where G is the selected voltage gain (Refer to Figure 1).

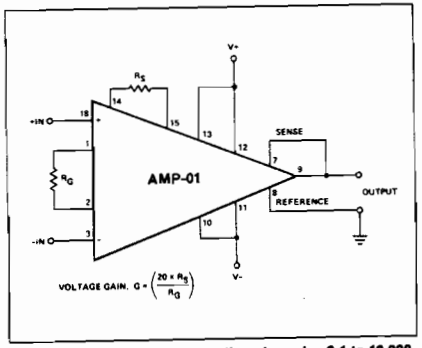
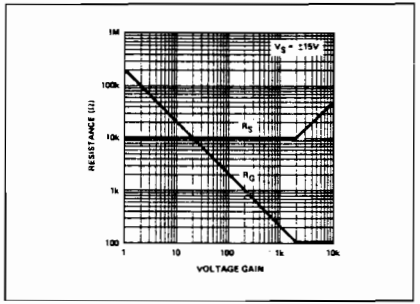


Figure 1. Basic AMP-01 connections for gains 0.1 to 10,000.

The magnitude of R_S affects linearity and output referred errors. Circuit performance is characterized using $R_S = 10k\Omega$ when operating on ±15 volt supplies and driving a ±10 volt output. R_S may be reduced to 5kΩ in many applications particularly when operating on ±5 volt supplies or if the output voltage swing is limited to ±5 volts. Bandwidth is improved with R_S = 5kΩ and this also increases common-mode rejection by approximately 6dB at low gain. Lowering the value below 5kΩ can cause instability in some circuit configurations and usually has no advantage. High voltage gains between two and ten thousand would require very low values of R_G. For $R_S = 10k\Omega$ and $A_V = 2000$ we get $R_G = 100\Omega$; this value is the practical lower limit for R_G. Below 100Ω, mismatch of wirebond and resistor temperature coefficients will introduce significant gain tempco errors. Therefore, for gains above 2,000, R_G should be kept constant at 100Ω and R_S increased. The maximum gain of 10,000 is obtained with R_S set to 50kΩ.

Metal-film or wirewound resistors are recommended for best results. The absolute values and TC's are not too important, only the ratiometric parameters.

AC amplifiers require good gain stability with temperature and time, but DC performance is unimportant. Therefore, low cost metal-film types with TC's of 50ppm/°C are usually adequate for R_S and R_G. Realizing the full potential of the AMP-01's offset voltage and gain stability requires precision metal-film or wirewound resistors. Achieving a 15ppm/°C gain tempco at all gains requires R_S and R_G temperature coefficient matching to 5ppm/°C or better.



R_G AND R_S SELECTION

Gain accuracy is determined by the ratio accuracy of R_S and R_G combined with the gain equation error of the AMP-01 (0.6% max for A/E grades).

All inatrumentation amplifiers require attention to layout so thermocouple effects are minimized. Thermocouples formed between copper and dissimilar metals can easily destroy the TCV_{OS} performance of the AMP-01 which is typically 0.15μV/°C. Resistors themselves can generate thermoelectric EMF's when mounted parallel to a thermal gradient. "Vishay" resistors are recommended because a maximum value for thermoelectric generation is specified. However, where thermal gradients are low and gain TC's of 20-50ppm are sufficient, general-purpose metal-film resistors can be used for R_G and R_S.

COMMON-MODE REJECTION

Ideally, an instrumentation amplifier responds only to the difference between the two input signals and rejects common-mode voltages and noise. In practice, there is a small change in output voltage when both inputs experience the same common-mode voltage change; the ratio of these voltages is called the common-mode gain. Common-mode rejection (CMR) is the logarithm of the ratio of differential-mode gain to common-mode gain, expressed in dB. CMR specifications are normally measured with a full-range input voltage change and a specified source resistance unbalance.

The current-feedback design used in the AMP-01 inherently yields high common-mode rejection. Unlike resistive feedback deaigns, typified by the three-op-amp IA, the CMR is not degraded by small resistances in series with the reference input. A slight, but trimmable, output offset voltage change results from resistance in series with the reference input.

The common-mode input voltage range, CMVR, for linear operation may be calculated from the formula:

$$CMVR = \pm\left(IVR - \frac{|V_{OUT}|}{2G}\right) \quad \text{(4)}$$

IVR is the data sheet specification for input voltage range; V_{OUT} is the maximum output signal; and G is the chosen voltage gain. For example, at 25°C, IVR is specified as ±10.5 volt minimum with ±15 volt supplies. Using a ±10 volt maximum swing output and substituting the figures in (4) simplifies the formula to:

$$CMVR = \pm\left(10.5 - \frac{5}{G}\right) \quad \text{(5)}$$

For all gains greater than or equal to 10, CMVR is ±10 volt minimum; at gains below 10, CMVR is reduced.

ACTIVE GUARD DRIVE

Rejection of common-mode noise and line pick-up can be improved by using shielded cable between the signal source and the IA. Shielding reduces pick-up, but increases input capacitance, which in turn degrades the settling-time for signal changes. Further, any imbalance in the source resistance between the inverting and noninverting inputs, when capacitively loaded, converts the common-mode voltage into a differential voltage. This effect reduces the benefits of shielding. AC common-mode rejection is improved by "bootstrapping" the input cable capacitance to the input signal, a technique called "guard driving". This technique effectively reduces the input capacitance. A single guard-driving signal is adequate at gains above 100 and should be the average value of the two inputs. The value of external gain resistor R_G is split between two resistors R_{G1} and R_{G2}; the center tap provides the required signal to drive the buffer amplifier (Figure 2).

GROUNDING

The majority of instruments and data acquisition systems have separate grounds for analog and digital signals. Analog ground may also be divided into two or more grounds which will be tied together at one point, usually the analog power-supply ground. In addition, the digital and analog grounds may be joined, normally at the analog ground pin on the A-to-D converter. Following this basic grounding practice is essential for good circuit performance (Figure 3).

Mixing grounds causes interactions between digital circuits and the analog signals. Since the ground returns have finite resistance and inductance, hundreds of millivolts can be developed between the system ground and the data acquisition components. Using separate ground returns minimizes the current flow in the sensitive analog return path to the system ground point. Consequently, noisy ground currents from logic gates do not interact with the analog signals.

Inevitably, two or more circuits will be joined together with their grounds at differential potentials. In these situations, the differential input of an instrumentation amplifier, with its high CMR, can accurately transfer analog information from one circuit to another.

SENSE AND REFERENCE TERMINALS

The sense terminal completes the feedback path for the instrumentation amplifier output stage and is normally connected directly to the output. The output signal is specified with respect to the reference terminal, which is normally connected to analog ground.

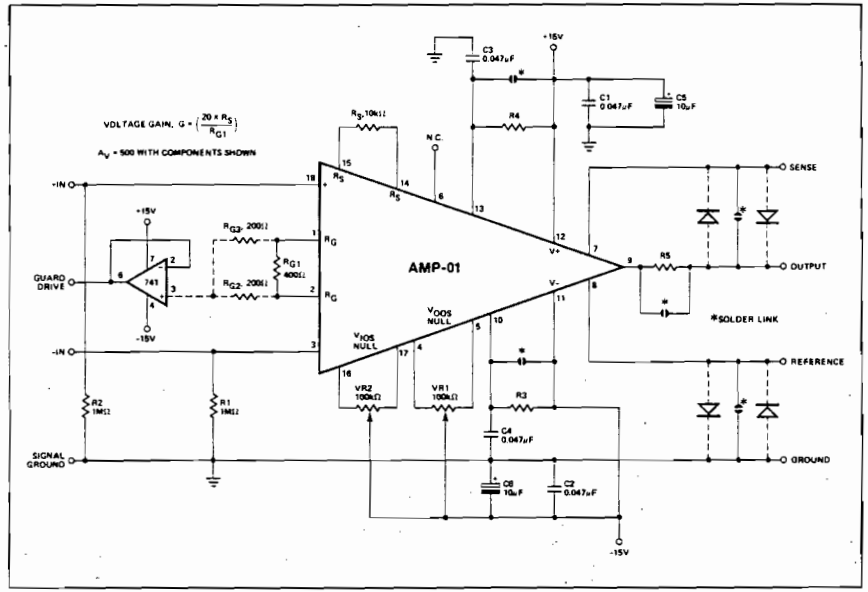


Figure 2. AMP-01 evaluation circuit showing guard-drive connection.

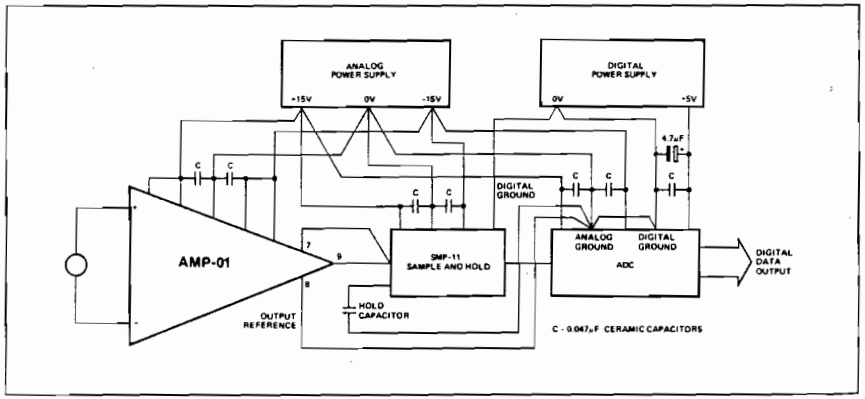


Figure 3. Basic grounding practice.

If heavy output currents are expected and the load is situated some distance from the amplifier, voltage drops due to track or wire resistance will cause errors. Voltage drops are particularly troublesome when driving 50Ω loads. Under these conditions, the sense and reference terminals can be used to "remote sense" the load as shown in Figure 4. This method of connection puts the IXR drops inside the feedback loop and virtually eliminates the error. An unbalance in the lead resistances from the sense and reference pins does not degrade CMR, but will change the output offset voltage. For example, a large unbalance of 3Ω will change the output offset by only 1mV.

DRIVING 50Ω LOADS

Output currents of 50mA are guaranteed into loads of up to 50Ω and 26mA into 500Ω. In addition, the output is stable and free from oscillation even with a high load capacitance. The combination of these unique features in an instrumentation amplifier allows low-level transducer signals to be conditioned and directly transmitted through long cables in voltage or current form. Increased output current brings increased internal dissipation, especially with 50Ω loads. For this reason, the power-supply connections are split into two pairs; pins 10 and 13 connect to the output stage only and pins 11 and 12 provide power to the input and following stages. Dual supply pins allow dropper resistors to be connected in series with the output stage so excess power is dissipated outside the package. Additional decoupling is necessary between pins 10 and 13 to ground to maintain stability when dropper resistors are used. Figure 5 shows a complete circuit for driving 50Ω loads.

HEATSINKING

To maintain high reliability, the die temperature of any IC should be kept as low as practicable, preferably below 100°C. Although most AMP-01 application circuits will produce very little internal heat — little more than the quiescent dissipation of 90mW — some circuits will raise that

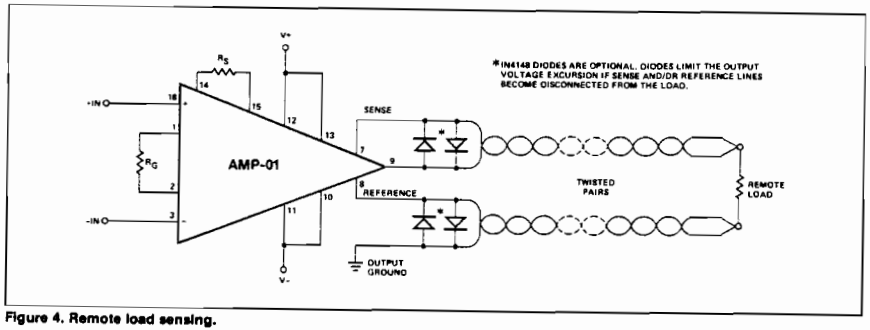


Figure 4. Remote load sensing.

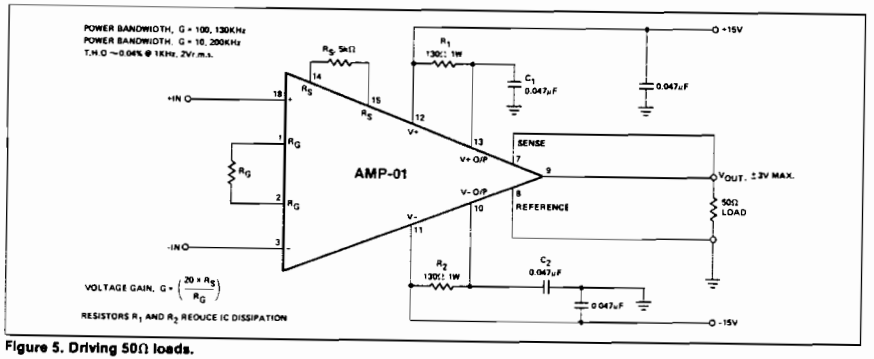


Figure 5. Driving 50Ω loads.

to several hundred milliwatts (for example, the 4-20mA current transmitter application, Figure 8). Excessive dissipation will cause thermal shutdown of the output stage thus protecting the device from damage. A heatsink is recommended in power applications to reduce the die temperature.

Several appropriate heatsinks are available; the Thermalloy 6010B is especially easy to use and is inexpensive. Intended for dual-in-line packages, the heatsink may be attached with a cyanoacrylate adhesive. This heatsink reduces the thermal resistance between the junction and ambient environment to approximately 80° C/W. Junction (die) temperature can then be calculated by using the relationship:

$$P_d = \frac{T_j - T_a}{\theta_{ja}}$$

where T_j and T_a are the junction and ambient temperatures respectively, θ_{ja} is the thermal resistance from junction to ambient, and P_d is the device's internal dissipation.

OVERVOLTAGE PROTECTION

Instrumentation amplifiers invariably sit at the front end of instrumentation systems where there is a high probability of exposure to overloads. Voltage transients, failure of a transducer, or removal of the amplifier power supply while the signal source is connected may destroy or degrade the performance of an unprotected amplifier. Although it is impractical to protect an IC internally against connection to power lines, it is relatively easy to provide protection against typical system overloads.

The AMP-01 is internally protected against overloads for gains of up to 100. At higher gains, the protection is reduced and some external measures may be required. Limited internal overload protection is used so that noise performance would not be significantly degraded.

AMP-01 noise level approaches the theoretical noise floor of the input stage which would be $4nV/\sqrt{Hz}$ at 1kHz when the gain is set at 1000. Noise is the result of shot noise in the input devices and Johnson noise in the resistors. Resistor noise is calculated from the values of R_G (200Ω at a gain of 1000) and the input protection resistors (250Ω). Active loads for the input transistors contribute less than $1nV/\sqrt{Hz}$ of noise. The measured noise level is typically $5nV/\sqrt{Hz}$.

Diodes across the input transistor's base-emitter junctions, combined with 250Ω input resistors and R_G, protect against differential inputs of up to ±20V for gains of up to 100. The diodes also prevent avalanche breakdown that would degrade the I_B and I_{OS} specifications. Decreasing the value of R_G for gains above 100 limits the maximum input overload protection to ±10V. External series resistors could be added to guard against higher voltage levels at the input, but resistors alone increase the input noise and degrade the signal-to-noise ratio, especially at high gains.

Protection can also be achieved by connecting back-to-back 9.1V zener diodes across the differential inputs. This technique does not affect the input noise level and can be used down to a gain of 2 with minimal increase in input current. Although voltage-clamping elements look like short circuits at the limiting voltage, the majority of signal sources provide less than 50mA, producing power levels that are easily handled by low-power zeners.

Simultaneous connection of the differential inputs to a low-impedance signal above 10V during normal circuit operation is unlikely. However, additional protection involves adding 100Ω current-limiting resistors in each signal path prior to the voltage clamp; the resistors increase the input noise level to just $5.4nV/\sqrt{Hz}$ (refer to Figure 6).

Input components, be they multiplexers or resistors, should be carefully selected to prevent the formation of thermocouple junctions which would degrade the input signal.

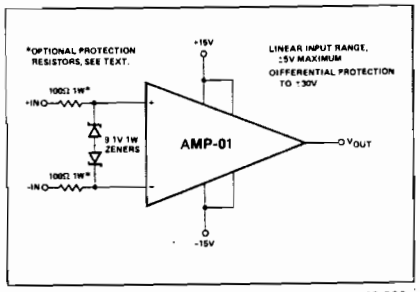


Figure 6. Input overvoltage protection for gains 2 to 10,000.

POWER SUPPLY CONSIDERATIONS

Achieving the rated performance of precision amplifiers in a practical circuit requires careful attention to external influences. For example, supply noise and changes in the nominal voltage directly affect the input offset voltage. A PSR of 80dB means that a change of 100mV on the supply, not an uncommon value, will produce a 10μV input offset change. Consequently, care should be taken in choosing a power unit that has a low output noise level, good line and load regulation, and good temperature stability.

APPLICATIONS INFORMATION

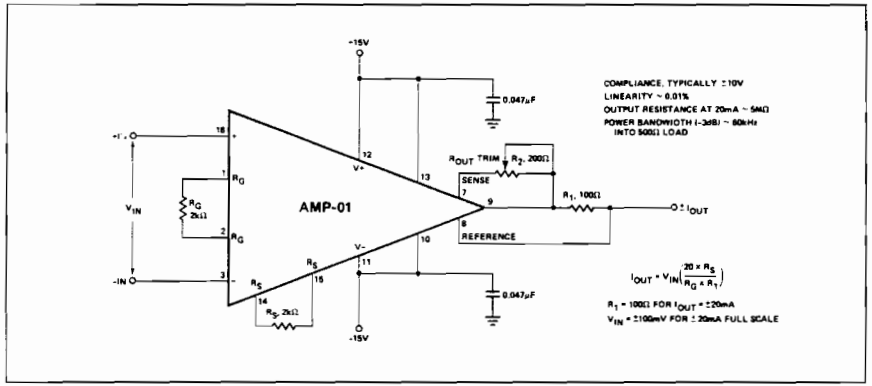


Figure 7. High-compliance bipolar current source with 13-bit linearity.

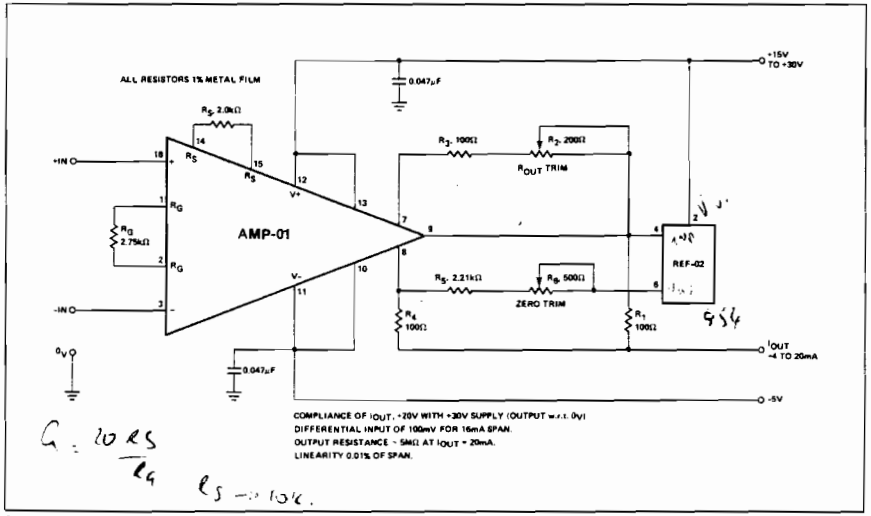


Figure 8. 13-bit linear 4-20mA transmitter constructed by adding a voltage reference. Thermocouple signals can be accepted without preamplification.

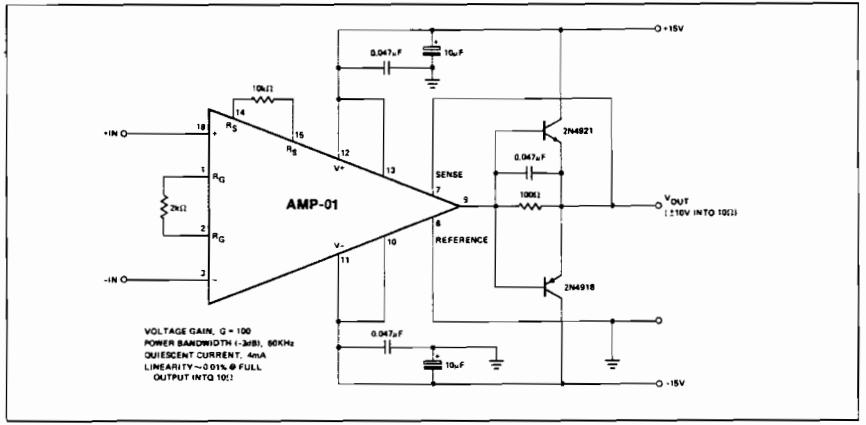


Figure 9. Adding two transistors increases output current to ± 1A without affecting the quiescent current of 4mA. Power bandwidth is 60kHz.

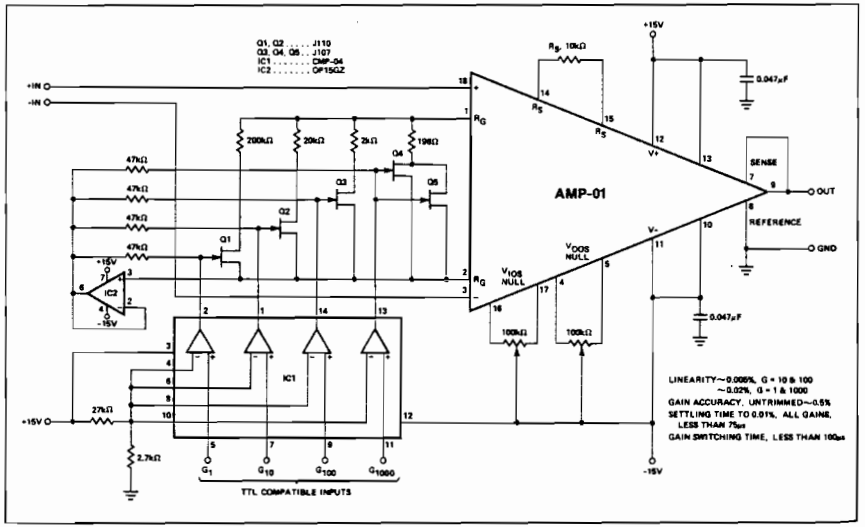


Figure 10. The AMP-01 makes an excellent programmable-gain instrumentation amplifier. Combined gain-switching and settling time to 13-bits falls below 100µs. Linearity is better than 12-bits over a gain range 1 to 1000.

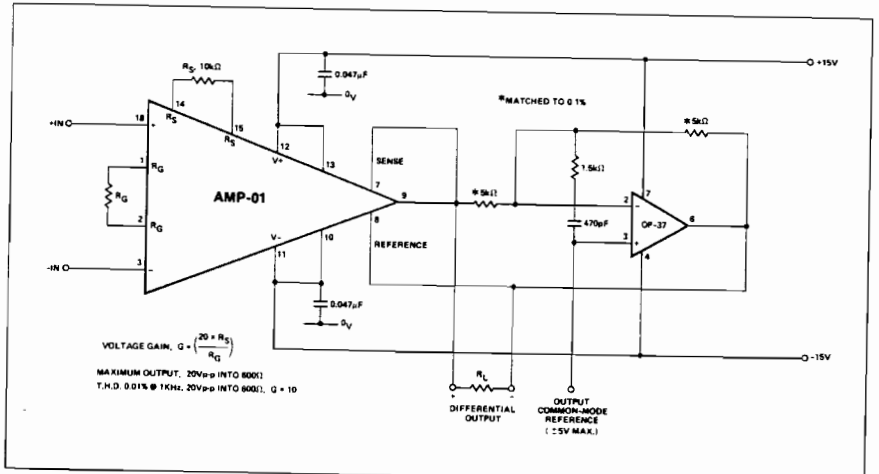


Figure 11. A differential input instrumentation amplifier with differential output replaces a transformer in many applications. The output will drive a 600Ω load at low distortion, (0.01%).

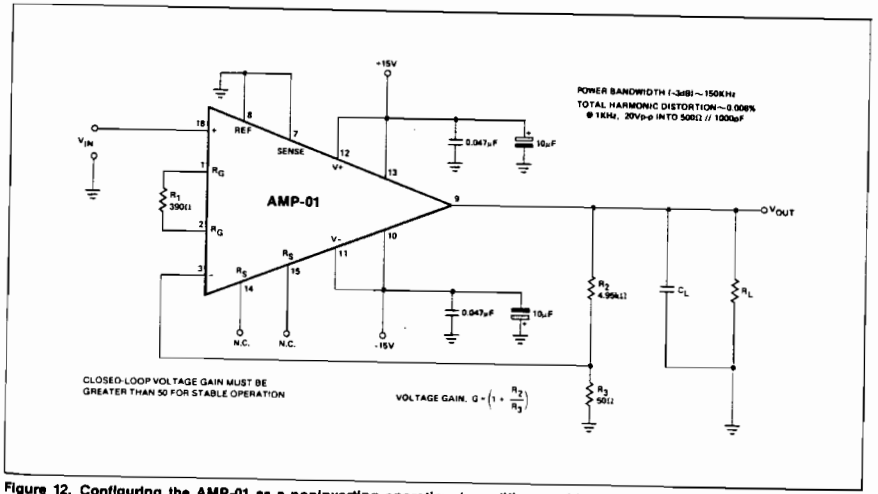


Figure 12. Configuring the AMP-01 as a noninverting operational amplifier provides exceptional performance. The output handles low load impedances at very low distortion, 0.006%.

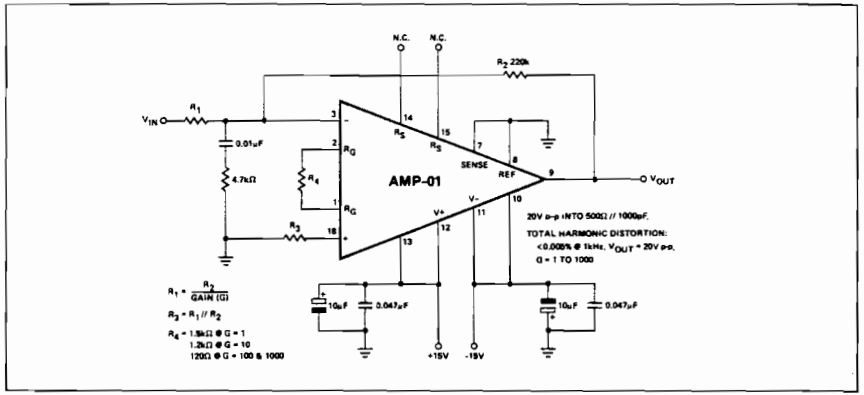


Figure 13. The inverting operational amplifier configuration has excellent linearity over the gain range 1 to 1000, typically 0.005%. Offset voltage drift at unity gain is improved over the drift in the instrumentation amplifier configuration.

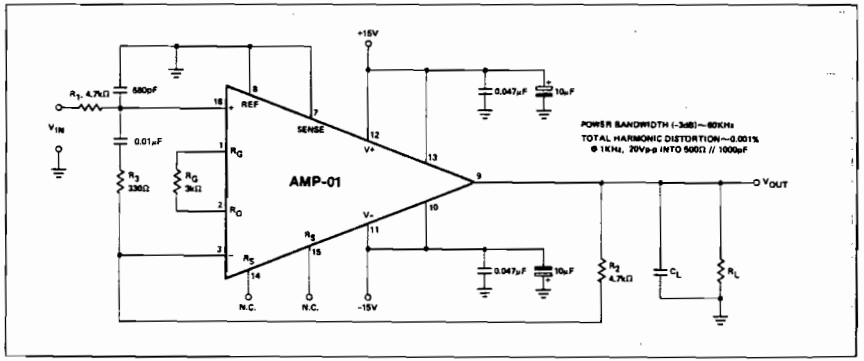
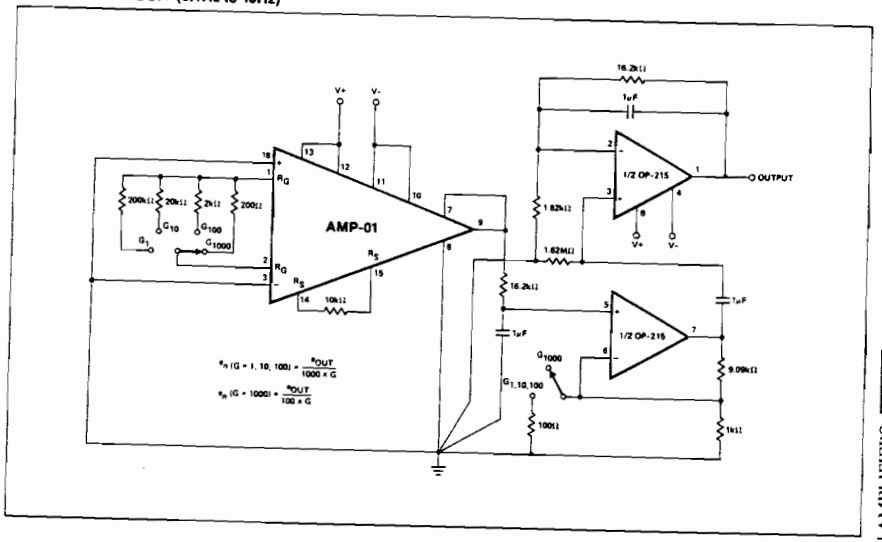
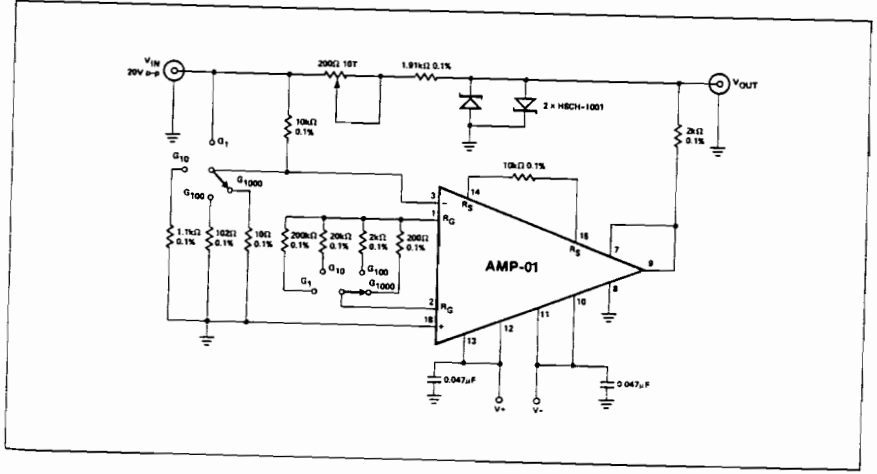


Figure 14. Stability with large capacitive loads combined with high output current capability make the AMP-01 ideal for line driving applications. Offset voltage drift approaches the TCV_{IOS} limit, (0.3μV/° C).

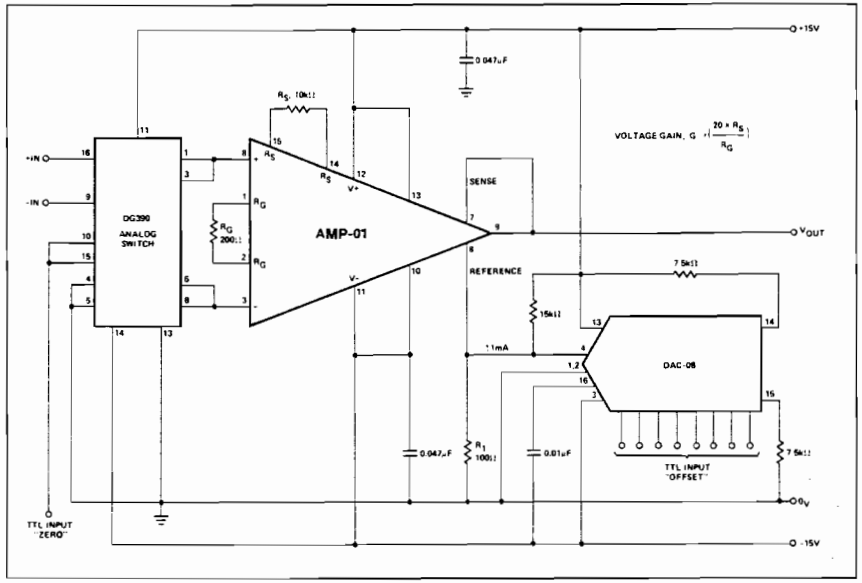
NOISE TEST CIRCUIT (0.1Hz to 10Hz)



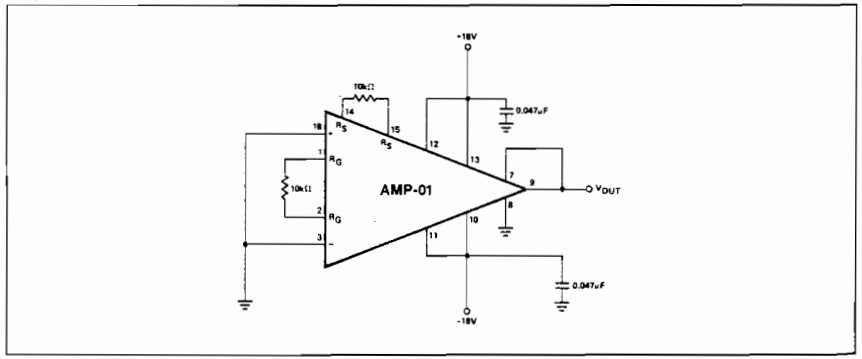
SETTLING-TIME TEST CIRCUIT



INSTRUMENTATION AMPLIFIER WITH AUTO-ZERO



BURN-IN CIRCUIT



AMP-02

HIGH ACCURACY 8-PIN INSTRUMENTATION AMPLIFIER

Precision Monolithics Inc.

FEATURES

- Low Offset Voltage ..... 100µV Max
- Low Drift ..... 2µV/°C Max
- Wide Gain Range ..... 1 to 10,000
- High Common-Mode Rejection ..... 115dB Min
- High Bandwidth (G = 1000) ..... 200kHz Typ
- Gain Equation Accuracy ..... 0.5% Max
- Single Resistor Gain Set
- Input Overvoltage Protection
- Low Cost
- Available in Die Form

APPLICATIONS

- Differential Amplifier
- Strain Gauge Amplifier
- Thermocouple Amplifier
- RTD Amplifier
- Programmable Gain Instrumentation Amplifier
- Medical Instrumentation
- Data Acquisition Systems

ORDERING INFORMATION †

T_A = +25°C V_{IOS} MAX (µV)	V_{OOS} MAX (mV)	PLASTIC 8-PIN	OPERATING TEMPERATURE RANGE
100	4	AMP02EP	XIND
200	8	AMP02FP	XIND

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages. For ordering information, see PMI's Data Book, Section 2.

GENERAL DESCRIPTION

The AMP-02 is the first precision instrumentation amplifier available in an 8-pin package. Gain of the AMP-02 is set by a single external resistor, and can range from 1 to 10,000. No gain set resistor is required for unity gain. The AMP-02 includes an input protection network that allows the inputs to be taken 60V beyond either supply rail without damaging the device.

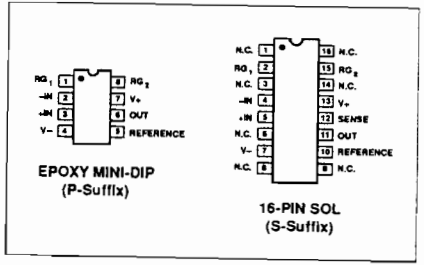
Laser trimming reduces the input offset voltage to under 100µV. Output offset voltage is below 4mV and gain accuracy is better than 0.5% for gain of 1000. PMI's proprietary thin-film resistor process keeps the gain temperature coefficient under 50 ppm/°C.

Due to the AMP-02's design, its bandwidth remains very high over a wide range of gain. Slew rate is over 4V/µs making the AMP-02 ideal for fast data acquisition systems.

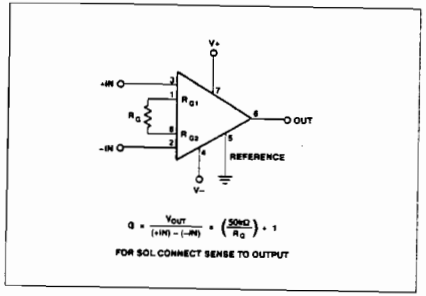
A reference pin is provided to allow the output to be referenced to an external DC level. This pin may be used for offset correction or level shifting as required. In the 8-pin package, sense is internally connected to the output.

For an instrumentation amplifier with the highest precision, consult the AMP-01 data sheet. For the highest input impedance and speed, consult the AMP-05 data sheet.

PIN CONNECTIONS



BASIC CIRCUIT CONNECTIONS



6 INSTRUMENTATION AMPLIFIERS